PCB DESIGN GUIDE 01

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PREPARING A PCB MANUFACTURING PACKAGE

WHY THE MANUFACTURING PACKAGE MATTERS

A PCB manufacturer can only build what is communicated. The release package must transfer design intent without relying on assumptions.

DESIGN INTENT
Complete and verified design data

CONTROLLED RELEASE
One controlled package with defined revision

CAM & DFM REVIEW
Manufacturing analysis and feedback

FABRICATION
Build to intent with controlled processes

INSPECTION & TEST
Verification and evidence of quality

CORE PRINCIPLE: Manufacturing data, fabrication drawing, stack-up, notes and purchase-order requirements must tell the same story.

WHAT A GOOD PACKAGE ACHIEVES

- Controls part number and revision
- Defines image, drill, mechanical and fabrication data
- States materials, thickness, copper and surface finish
- Identifies impedance structures and test requirements
- Defines all special processes
- States acceptance evidence and documentation
- Enables engineering queries before production

MINIMUM	PRODUCTION-READY	HIGH-RELIABILITY
Gerber/ODB++ • Drill data • Outline • Basic notes	Data • Drawings • Stack-up • Impedance • Netlist • Clear notes	Production-ready package plus standards • Coupons • Reports • Traceability • Change control
Simple prototypes and low-risk boards	Repeat production and industrial designs	Defence, aerospace and mission-critical products

ONE CONTROLLED ZIP ARCHIVE • ONE PART NUMBER • ONE REVISION • NO PIECEMEAL RELEASES

PREPARING A PCB MANUFACTURING PACKAGE

RELEASE CONTENTS • DATA FORMATS • LAYER SET

Agree one primary manufacturing-data format with the fabricator and identify it as the manufacturing master.

01_FAB_DATA

Gerber X2/X3, ODB++Design or IPC-2581

02_DRILL_ROUTE

PTH, NPTH, rout, slots and depth data

03_DRAWINGS

Fabrication, drill, outline and panel drawings

04_STACKUP

Layers, materials, copper and dielectrics

05_IMPEDANCE

Targets, geometries and coupon requirements

06_NETLIST

IPC-D-356 or equivalent extracted netlist

07_SPECIFICATIONS

Customer, IPC and special-process requirements

08_README

Revision, file list and release instructions

FORMAT SELECTION

GERBER
Modern attributed image data

ODB++DESIGN
Intelligent structured manufacturing data

IPC-2581
Intelligent neutral exchange when supported

DO NOT CREATE MULTIPLE MASTERS.
If several formats are supplied, explicitly identify the controlling data set.

RECOMMENDED LAYER SET

- **Copper** — Top, all internal layers, bottom
- **Solder mask** — Top and bottom
- **Legend** — Top and bottom as required
- **Profile** — One authoritative finished outline
- **Drill** — PTH, NPTH and special structures
- **Job / attributes** — Include when generated

PASTE DATA IS NORMALLY ASSEMBLY DATA—DO NOT CONFUSE IT WITH SOLDER MASK.

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FABRICATION DRAWING • STACK-UP • IMPEDANCE

The fabrication drawing is the human-readable contract for the bare board; the stack-up is both a mechanical and electrical definition.

FABRICATION DRAWING — DEFINE

- Part number, PCB name and revision
- Finished dimensions, datum and tolerances
- Finished thickness and layer count
- Material and copper requirements
- Surface finish, solder mask and legend
- PTH, NPTH, slots and special holes
- Impedance table and controlled layers
- Backdrill, via fill, edge plating and press-fit
- Standard, class, electrical test and coupons
- Marking, serialization and traceability

STACK-UP — FOR EACH LAYER

- Layer number and functional name
- Signal, plane or mixed-layer function
- Starting / finished copper
- Core, prepreg and dielectric thickness
- Laminate family and electrical properties
- Copper foil type where performance-critical
- Associated impedance structures
- Sequential lamination or HDI cycles

NET / CLASS	PCIe_TX • 1000BASE-T • LVDS_CLK • RF_50R
TARGET	50 Ω single-ended • 90 Ω or 100 Ω differential
TOLERANCE	Define project requirement
LAYER	Identify signal and reference planes
GEOMETRY	Trace width and differential spacing
COUPON / REPORT	State coupon and TDR requirements

HIGH-SPEED CAUTION: Verify dielectric thickness, copper thickness, roughness assumptions, solder-mask influence and the manufacturer's Dk model—not trace width alone.

Any manufacturer-proposed stack-up must preserve electrical, mechanical, material and reliability constraints and receive formal approval.

PREPARING A PCB MANUFACTURING PACKAGE

DRILLS • MECHANICAL • MATERIALS • ELECTRICAL TEST

01 DRILL, VIA & HOLE DEFINITION

- Separate PTH and NPTH data
- State finished-hole size and tolerance
- Separate blind, buried, laser and controlled-depth drills
- Identify via-in-pad, filled, capped, plugged or tented vias
- Define backdrill start, stop, target stub and tolerance
- Define press-fit finished-hole requirements
- Identify plated and non-plated slots
- Do not pre-compensate drills for plating unless agreed

TENTED • PLUGGED • FILLED • RESIN-FILLED • CAPPED • PLATED-OVER ARE NOT INTERCHANGEABLE

02 MECHANICAL & PROFILE

- One authoritative board outline
- Units and coordinate origin
- Slots, cut-outs, radii and edge tolerances
- V-score, tab-route and breakaways when controlled
- Bevels, gold fingers and connectors
- Edge plating and castellations
- Critical connector-to-edge and mounting tolerances

03 MATERIAL & SURFACE FINISH

- Define FR-4, high-Tg, low-loss, RF or polyimide requirements
- Control Tg, Td, Dk/Df, CAF, moisture and compliance where relevant
- Specify ENIG, ENEPIG, immersion silver/tin, OSP, HASL or hard gold
- Define selective finish and thickness where critical

04 NETLIST & ELECTRICAL TEST

- 100% electrical test requirement
- Independent IPC-D-356 netlist where practical
- Continuity and isolation criteria
- Flying-probe, fixture or agreed method
- Required report or certificate

A test against CAM data regenerated from the same incorrect interpretation may confirm consistency—not design intent.

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PREPARING A PCB MANUFACTURING PACKAGE

QUALITY EVIDENCE • REVISION CONTROL • RELEASE VERIFICATION

QUALITY EVIDENCE — DEFINE BEFORE QUOTATION

Certificate of Conformity	Part • Revision • Lot • Applicable specification
Electrical test	Pass confirmation or agreed report
Controlled impedance	TDR / coupon report
Microsection	Cross-section images and measurements
Material traceability	Laminate / prepreg certificate or lot
Dimensional inspection	FAI or critical-dimension report
Surface finish	Thickness report when required
Solderability / cleanliness	Process or laboratory report
Lot traceability	Date code, lot, traveler or production record

README & REVISION CONTROL

- Customer / project
- PCB part number and revision
- Release date and purpose
- Primary manufacturing-data format
- Included files and folders
- Drawing and stack-up revision
- Special processes and critical requirements
- Reports, certificates and approved deviations
- Engineering contact

EXAMPLE PACKAGE NAME:

NP-12345_REV-C_PCB-FAB_2026-08-12.zip

NEVER OVERWRITE AN OLD RELEASE USING THE SAME FILENAME.

INDEPENDENT PRE-RELEASE VERIFICATION

- View final exported data independently
- Verify layer count, order, polarity and alignment
- Overlay copper, mask and drills
- Check outline, slots and cut-outs
- Confirm PTH / NPTH separation
- Review drill sizes and via treatments
- Check legend and solder-mask openings
- Compare drawing, stack-up and impedance data
- Confirm netlist and final ZIP contents

TWO-SOURCE VERIFICATION:
Compare critical information using independent sources wherever practical.

NOVATRONIC PCB

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COMMON MISTAKES • DFM CONTROL • FINAL CHECKLIST

MISTAKE	BETTER PRACTICE
Conflicting outlines	Provide one authoritative profile
Generic layer names	Use attributes and a clear stack-up
Missing NPTH distinction	Separate plated and non-plated data
Impedance note without structure	Provide targets, layers, geometry and tolerance
No press-fit hole tolerance	Define finished hole and tolerance
Material stated only as FR-4	Define performance or approved material
Contradictory revisions	Use one controlled release archive
Special process only in email	Place it in controlled data and drawings
No independent output review	Review final manufacturing outputs
Unclear acceptance documents	Define evidence at RFQ / PO stage

FINAL RELEASE CHECK

- ☐ Part number and revision agree everywhere
- ☐ Primary manufacturing format identified
- ☐ Copper, mask, legend, profile and drill data complete
- ☐ Fabrication drawing and stack-up current
- ☐ Materials, thickness and finish defined
- ☐ Impedance targets and coupons defined
- ☐ Special processes fully specified
- ☐ Standards, class and electrical test defined
- ☐ Reports, certificates and traceability defined
- ☐ Exported data independently checked
- ☐ Final ZIP opened and verified
- ☐ Manufacturer instructed to raise queries before changes

DISCIPLINED EQ / DFM PROCESS

1. Manufacturer raises a numbered item
2. Technical impact is assessed
3. Proposed change is checked against requirements
4. Customer approval is obtained where required
5. Response is recorded against the job revision
6. Production starts only after critical items close

NO SILENT CHANGES TO STACK-UP, TRACE GEOMETRY, FINISHED HOLES, MATERIAL, SURFACE FINISH OR OTHER CONTROLLED FEATURES.

REMOVE UNCERTAINTY • CONTROL THE DATA • QUALIFY THE FABRICATION ROUTE • PRESERVE OBJECTIVE EVIDENCE