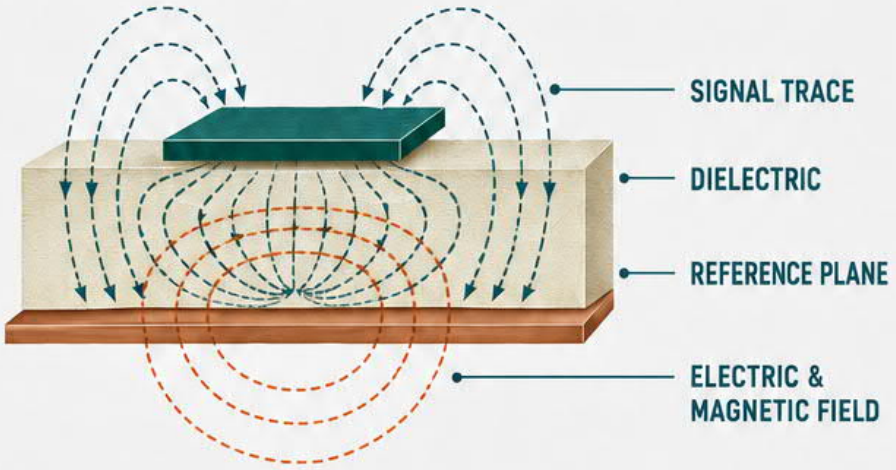
CONTROLLED-IMPEDANCE BASICS

TRANSMISSION-LINE FUNDAMENTALS • WHY IT MATTERS

When an interconnect becomes electrically long relative to signal transition time, the trace, reference conductor and dielectric form a transmission line with characteristic impedance Z_0.



KEY IDEA

IMPEDANCE IS NOT A PROPERTY OF THE TRACE ALONE.

IT BELONGS TO THE COMPLETE ELECTROMAGNETIC STRUCTURE.

WHY DESIGNERS CARE

- Reflections distort edges and reduce timing margin
- Overshoot and undershoot can increase
- Differential links need predictable differential and common-mode behaviour
- RF circuits depend on matching and controlled power transfer
- Fast edge rate and interconnect length increase sensitivity

TYPICAL NOMINAL ORIENTATION

GENERAL DIGITAL	50 Ω single-ended
USB	Often 90 Ω differential
PCI EXPRESS	Commonly 85 Ω differential at PCB level
ETHERNET	Often 100 Ω differential
LVDS	Typically 100 Ω differential
RF / MICROWAVE	Commonly 50 Ω single-ended

USE THE APPLICABLE COMPONENT, INTERFACE OR SYSTEM SPECIFICATION—NOT A GENERIC TABLE.

WHEN TO CONSIDER TRANSMISSION-LINE EFFECTS

- Compare one-way propagation delay with signal rise / fall time
- Edge rate is usually more useful than clock frequency alone

DC RESISTANCE

Steady current • Copper length and cross-section

CHARACTERISTIC IMPEDANCE Z_0

Travelling wave • Geometry, reference and dielectric

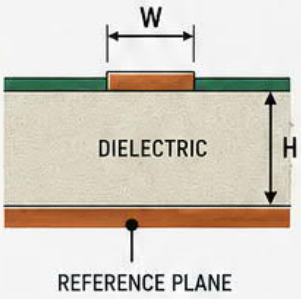
$$Z_0 \approx \sqrt{\frac{L'}{C'}}$$

CONTROLLED-IMPEDANCE BASICS

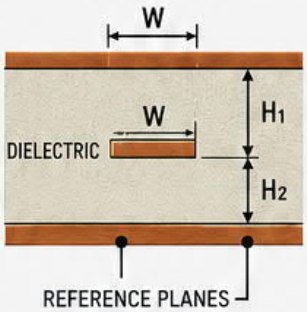
TRANSMISSION-LINE STRUCTURES • GEOMETRY VARIABLES

Trace width, copper thickness, spacing, dielectric height, Dk, solder mask and copper roughness combine to determine impedance.

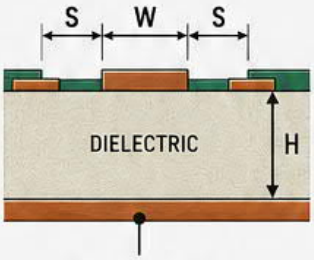
MICROSTRIP –
Outer trace referenced to plane below



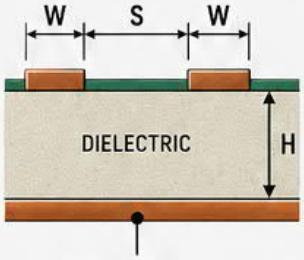
STRIPLINE –
Inner trace between reference planes



GROUNDED COPLANAR –
Adjacent same-layer ground plus reference plane

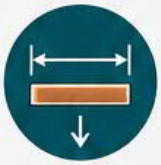


DIFFERENTIAL PAIR –
Two coupled conductors and reference environment



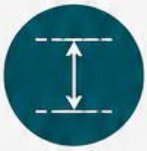
SEVEN KEY VARIABLES AND THEIR TYPICAL IMPACT ON IMPEDANCE

TRACE WIDTH



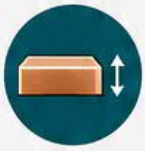
TRACE WIDTH ↑
→ Z_0 generally ↓

DIELECTRIC HEIGHT



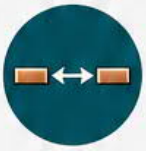
DIELECTRIC HEIGHT ↑
→ Z_0 generally ↑

COPPER THICKNESS



COPPER THICKNESS
→ changes conductor geometry

PAIR SPACING



PAIR SPACING
→ changes coupling and Z_{diff}

Dk



Dk ↑
→ Z_0 generally ↓

SOLDER MASK



SOLDER MASK
→ shifts outer-layer impedance

COPPER ROUGHNESS



COPPER ROUGHNESS
→ affects high-frequency loss and behaviour

REAL PRODUCTION GEOMETRY



Outer copper includes plating effects



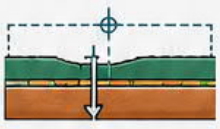
Etched conductors are not perfect rectangles



Prepreg thickness changes after lamination



Dk depends on construction, frequency and test method



Mask thickness and registration vary

THE SAME TRACE WIDTH CAN PRODUCE DIFFERENT IMPEDANCE ON DIFFERENT LAYERS.

USE A FIELD SOLVER AND THE FABRICATOR'S ACTUAL MATERIAL / PROCESS MODEL FOR PRODUCTION.

PCB DESIGN GUIDE 03

CONTROLLED-IMPEDANCE BASICS

DIFFERENTIAL PAIRS • RETURN PATHS • VIAS

A controlled route includes its reference environment and every transition—not only its uniform trace sections.

FOUNDATION • BUILDING BLOCKS • ENGINEERING IMPACT

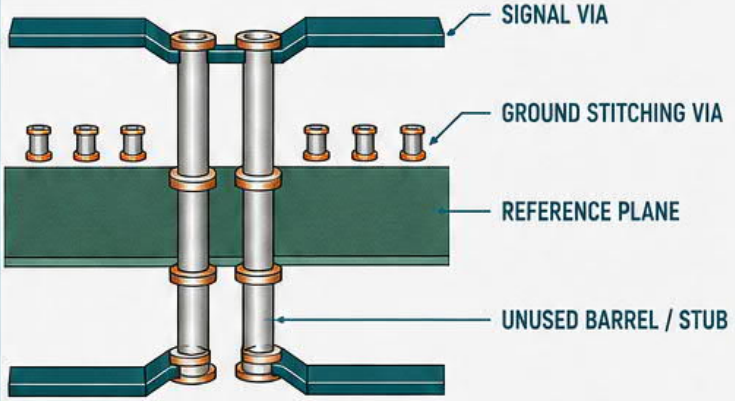
SINGLE-ENDED Z_0	One conductor referenced to plane(s)	Example: 50 Ω
DIFFERENTIAL Z_{diff}	Two coupled conductors driven oppositely	Example: 90 Ω / 100 Ω
ODD-MODE IMPEDANCE	Per-line modal impedance under differential excitation	Related to, but not interchangeable with, isolated Z_0
COMMON-MODE IMPEDANCE	Both lines move together	Relevant to EMI and mode conversion

TWO INDIVIDUALLY 50 Ω TRACES DO NOT AUTOMATICALLY FORM A 100 Ω DIFFERENTIAL PAIR.

REFERENCE PLANES & RETURN CURRENT

- Route critical traces over continuous references
- Avoid plane splits, slots and large voids
- Keep reference interruptions away from controlled routes
- Treat connector launches and layer changes as part of the path
- Provide a deliberate return transition when references change

TYPICAL LAYER TRANSITION (TOP TO INNER)



VIA & DISCONTINUITY EFFECTS



PERFECT NOMINAL TRACE WIDTH CANNOT COMPENSATE FOR A BROKEN RETURN PATH.

CONTROLLED-IMPEDANCE BASICS

Design-stage calculations establish sensible geometry; the selected manufacturer must confirm the actual production construction and compensation.

FIELD SOLVING • MANUFACTURER COLLABORATION • TOLERANCE



DESIGNER PROVIDES

- Nominal impedance target
- Allowed tolerance
- Single-ended or differential
- Signal layer and reference plane(s)
- Nominal width and differential spacing
- Material restrictions or approved family
- Finished thickness and copper
- Permission rules for width / spacing adjustment
- Coupon and report requirements

MANUFACTURER RETURNS

- Proposed production stack-up
- Actual core / prepreg constructions
- Material manufacturer and grade
- Calculated production width and spacing
- Finished copper assumptions
- Calculated impedance
- Expected manufacturing tolerance
- Coupon design and test method
- Required changes or exceptions

TOLERANCE BUDGET – KEY FACTORS INFLUENCING IMPEDANCE

TRACE WIDTH	Etch / imaging variation	Changes Z_0
COPPER THICKNESS	Foil + plating variation	Changes geometry
DIELECTRIC THICKNESS	Prepreg flow / pressing	Changes reference distance
Dk	Material / construction / frequency	Changes velocity and Z_0
PAIR SPACING	Imaging / etch tolerance	Changes Z_{diff}
SOLDER MASK	Thickness / registration	Shifts outer-layer Z_0

ANY CHANGE TO IMPEDANCE-CRITICAL WIDTH OR SPACING MUST BE CHECKED AGAINST CLEARANCES, COUPLING, BREAKOUTS AND CONNECTOR LAUNCHES.

Validate impedance early, document assumptions, and follow the manufacturer's process.

CONTROLLED-IMPEDANCE BASICS

COUPONS •
TDR •
FABRICATION NOTES •
MATERIAL EFFECTS

Objective impedance verification requires a representative production coupon, a defined measurement method and lot-level traceability.

CONTROLLED-IMPEDANCE COUPON

- Fabricated on the production panel
- Uses the same controlled-Z layer
- Represents dielectric construction and copper condition
- Uses representative width / spacing
- Provides adequate test-line length
- Maintains traceability to the board lot
- Customer-defined, IPC-derived or manufacturer-standard by agreement

TDR MEASUREMENT PROCESS

FAST EDGE → COUPON LAUNCH → TEST LINE → REFLECTION RESPONSE → IMPEDANCE PROFILE

TDR MEASUREMENT DEPENDS ON

- Calibration
- Probe / fixture and launch quality
- Coupon length
- Measurement bandwidth
- Analysis window
- Reporting method

DO NOT OVER-INTERPRET A SINGLE NUMBER.
COUPON DESIGN, LAUNCH REGION, WINDOW AND TEST SYSTEM MATTER.

FABRICATION DRAWING — DEFINE

- ID Impedance ID
- Layer
- Single-ended or differential type
- Target and tolerance
- Nominal design geometry
- Reference plane(s)
- Coupon requirement
- Test-report requirement

IMPEDANCE ID	LAYER	TYPE	TARGET IMPEDANCE	TOLERANCE	REFERENCE PLANE(S)
Z1	L1	Single-ended	50 Ω	±10%	L2 GND
Z2	L3	Differential	100 Ω	±10%	L2 & L4 GND

ILLUSTRATIVE ONLY — PRODUCTION DIMENSIONS REQUIRE THE ACTUAL MATERIAL CONSTRUCTION.

HIGH-SPEED MATERIAL EFFECTS

- Dk — Dk — Impedance and propagation velocity
- Df — Df — Dielectric loss
- Copper roughness — Conductor loss
- Glass weave — Local skew and impedance variation

Approved production stack-up and impedance reports belong in the controlled manufacturing record.

NOVATRONIC PCB

PCB DESIGN GUIDE 03

VISUAL GUIDE • SHEET 6 OF 6

CONTROLLED-IMPEDANCE BASICS

FOUNDATION • BUILDING BLOCKS • ENGINEERING IMPACT

COMMON MISTAKES • DESIGN WORKFLOW • FINAL REVIEW

COMMON DESIGN MISTAKES

CLOCK FREQUENCY USED INSTEAD OF EDGE RATE	→ Consider rise / fall time and interconnect delay
ROUTING OVER PLANE SPLITS	→ Use continuous references
2 × 50 Ω ASSUMED TO BE 100 Ω DIFF	→ Solve the actual coupled geometry
FINISHED COPPER IGNORED	→ Use fabricator finished-copper assumptions
GENERIC FR-4 Dk	→ Use appropriate laminate design data
SOLDER MASK IGNORED	→ Include mask in the outer-layer model
LONG VIA STUBS	→ Review layer assignment and backdrill
NO COUPON / TEST REQUIREMENT	→ Specify verification where required
WIDTH CHANGED WITHOUT APPROVAL	→ Use a controlled EQ / change process
UNJUSTIFIED TIGHT TOLERANCE	→ Set tolerance from the system budget

PRACTICAL DESIGN WORKFLOW

1. Identify controlled interfaces from specifications
2. Select layer count and reference strategy
3. Choose realistic materials and dielectrics
4. Estimate geometry using a field solver
5. Confirm routability and manufacturability
6. Route over continuous references and control transitions
7. Submit stack-up and impedance table to fabricator
8. Review proposed production construction
9. Approve all changes before manufacture
10. Require coupon / TDR evidence where applicable
11. Archive approved data and results

FINAL CONTROLLED-IMPEDANCE REVIEW

- [ ] Targets and tolerance come from applicable specifications
- [ ] Single-ended and differential structures are distinguished
- [ ] Layers and reference planes are defined and continuous
- [ ] Material Dk and finished copper assumptions are documented
- [ ] Mask, differential coupling and critical neck-downs are modelled
- [ ] Vias, launches, stubs and return transitions are reviewed
- [ ] Manufacturer adjustment authority is explicitly controlled
- [ ] Production stack-up and geometry are approved
- [ ] Coupon and TDR reporting requirements are defined
- [ ] Test results are traceable to the manufactured lot

DEFINE THE ELECTRICAL REQUIREMENT • ENGINEER THE STRUCTURE
CONTROL CHANGES • VERIFY THE RESULT