VIA TYPES AND MANUFACTURING CONSIDERATIONS

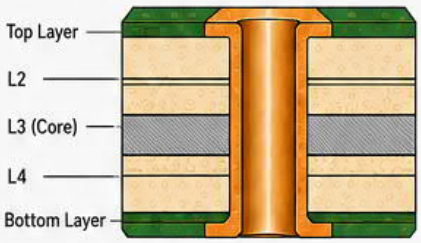
PURPOSE • VIA FAMILIES • SELECTION ///

Choose the Simplest Structure That Meets the Requirement

LEAD PRINCIPLE: Every additional lamination, drilling, filling or plating step affects cost and process risk.

1 PLATED THROUGH VIA (PTH)

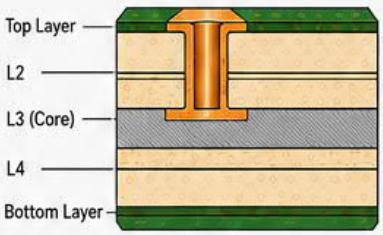
Outer to outer, mechanically drilled.



- Mature and lowest complexity
- Mechanically drilled and plated
- Consumes routing space on every penetrated layer

2 BLIND VIA

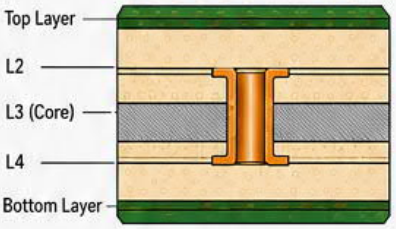
Outer layer to internal layer; mechanical or laser.



- Improves escape density
- Does not reach the opposite side
- Build sequence matters

3 BURIED VIA

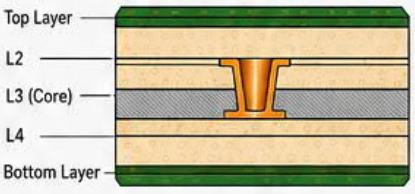
Internal to internal; formed before final lamination.



- Frees outer layers for routing
- Formed before final lamination
- Adds subassembly processing

4 MICROVIA

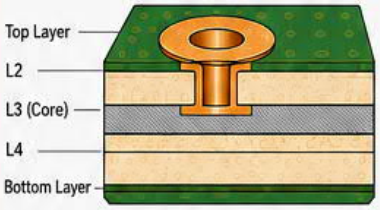
Usually through a thin dielectric; commonly laser formed.



- High density interconnect solution
- Typically laser drilled
- Reliability depends on geometry and process control

5 VIA-IN-PAD

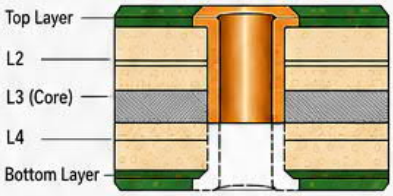
Via inside component land; excellent escape or thermal path.



- Provides escape or heat transfer
- Solderable pads require controlled fill / planarize / cap
- Ensures reliability and solder joint quality

6 BACKDRILLED VIA

Unused plated barrel removed by controlled-depth drilling.



- Reduces signal stub and reflections
- Improves high-speed performance
- Requires depth control and registration accuracy

Soldermask | Copper | Prepreg (Dielectric) | Core | Plated Via Barrel

SELECT BY PURPOSE

LAYERS TO CONNECT
- PTH: outer to outer
- Blind: outer to inner
- Buried: inner to inner
- Microvia: thin dielectric
- Backdrilled PTH: outer to outer with stub removal

ROUTING DENSITY
- Use microvias and blind vias to increase escape density
- Via-in-pad to minimize breakout congestion

HIGH SPEED SIGNALS
- Minimize stubs: use backdrilling
- Avoid unnecesary layer transitions
- Follow geometry, antipad and reference rules

CURRENT / HEAT
- Use PTH or via-in-pad for current return and thermal performance
- Increase via count or barrel size

COMPONENT PAD
- Via-in-pad for BGAs, LGA, QFN or thermal pads
- Ensure controlled fill/planarize/cap for solderable surfaces

PROTECTION / FILL
- Filled & capped vias provide flat, reliable surfaces
- Select conductive or non-conductive fill as required

INSPECTION & PRODUCT CLASS
- Higher class products need tighter control
- Verify capability for build sequence, drill, plate, fill and backdrill

Complexity must be introduced deliberately — not as a routing afterthought.

Choose the simplest via structure that meets the electrical, thermal and mechanical requirement.

VIA TYPES AND MANUFACTURING CONSIDERATIONS

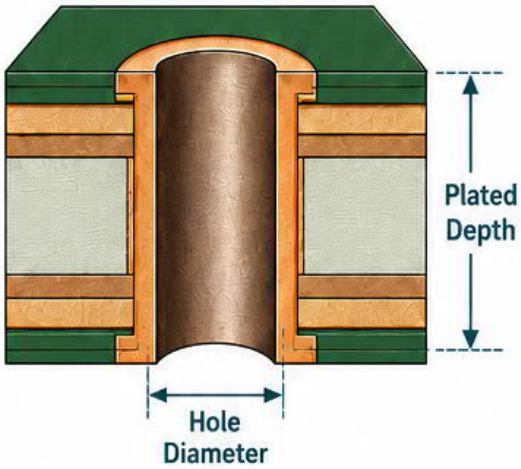
ASPECT RATIO • FINISHED HOLE • ANNULAR RING

1 ASPECT RATIO

Aspect ratio = plated depth ÷ hole diameter

Increasing aspect ratio makes desmear, activation and uniform barrel plating harder—raising the risk of thin plating at the center of the barrel.

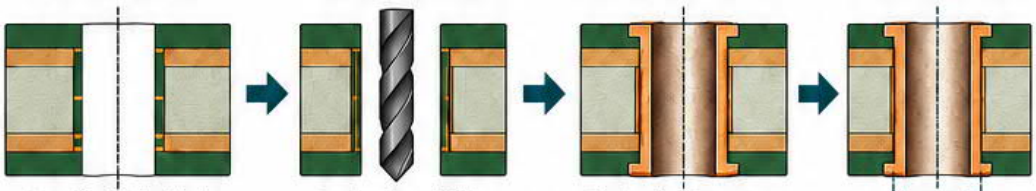
- Thin plating risk at center of barrel
- Drill-smear and voids can reduce reliability



KEY CONSIDERATIONS

- Desmear effectiveness decreases with depth.
- Activation coverage is harder to maintain.
- Plating distribution may thin toward the center of the barrel.

2 DRILL SIZE ≠ FINISHED HOLE



Specify finished hole and tolerance.

Production drill is generally larger than the required finished opening.

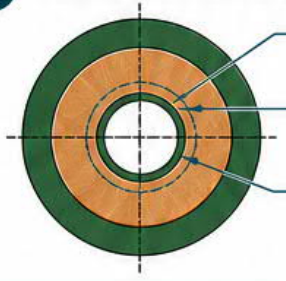
Plating builds copper to the finished size.

Finished hole meets specified size and tolerance.

For critical press-fit, connector and leaded holes, specify finished hole and tolerance.

Let the fabricator apply drill compensation.

3 ANNULAR RING & REGISTRATION



Drill wander and registration errors reduce annular ring.

Pad diameter, via diameter, artwork registration, plating and layer alignment must be engineered together.

- Soldermask Opening (Top View)
- Pad (Copper)
- Nominal Hole (Artwork)
- Worst Case Hole (After Wander)
- Finished Hole (After Plating)

HOLE GEOMETRY CHECKLIST

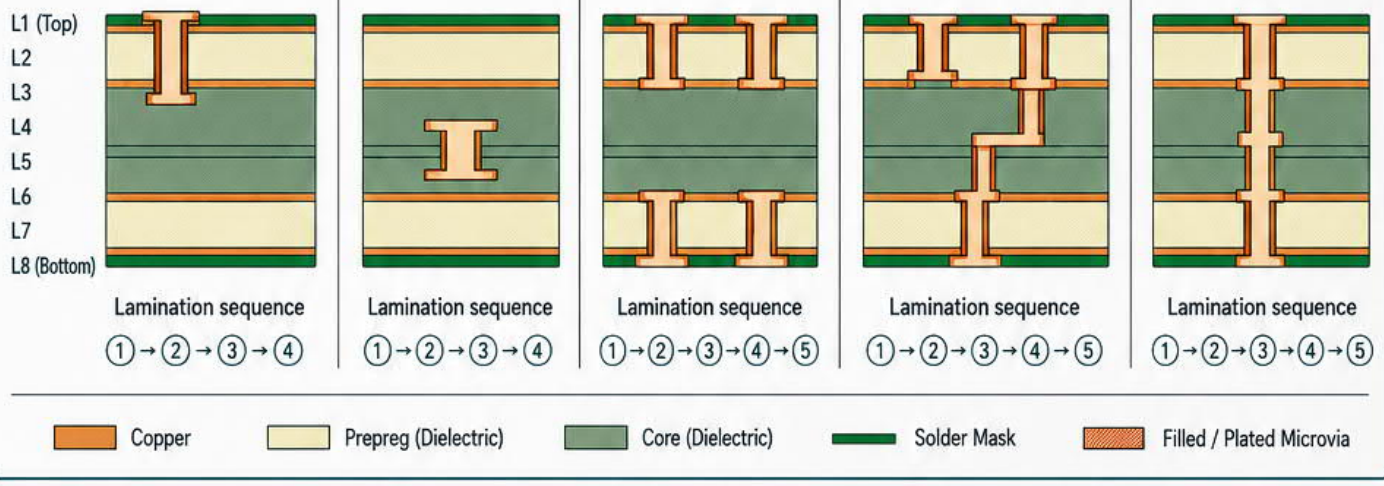
- [x] Board thickness and layer count defined
- [x] Material type and copper weight confirmed
- [x] Finished hole size and tolerance specified
- [x] Plating requirement (through-hole / via) defined
- [x] Supplier process window understood
- [x] Product class and field reliability considered

DO NOT USE ONE UNIVERSAL ASPECT-RATIO LIMIT.
Evaluate based on board thickness, materials, process capability and product reliability needs.

NOMINAL PAD-TO-HOLE GEOMETRY ALONE DOES NOT PROVE FINISHED ANNULAR RING.
Account for drill wander, registration, plating build and layer alignment.

VIA TYPES AND MANUFACTURING CONSIDERATIONS

BLIND • BURIED • HDI • MICROVIA RELIABILITY



WHY HDI IS USED

FINE-PITCH BGA ESCAPE
Escape more balls in a smaller area.

SMALLER PADS & ANTI-PADS
Enables reduced pad and annular ring sizes.

MORE ROUTING CHANNELS
Increases routing capacity within the same footprint.

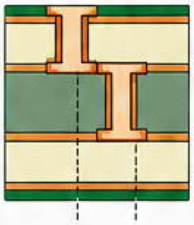
SHORTER VERTICAL INTERCONNECTS
Improves signal integrity and reduces stub length.

VIA-IN-PAD CAPABILITY
Supports dense BGA and fine-pitch interconnects.

SEQUENTIAL-BUILD ARCHITECTURES
Builds complexity layer-by-layer for maximum density.

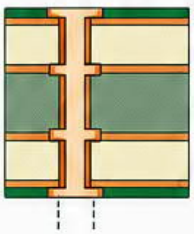
STAGGERED VS STACKED

STAGGERED (LATERALLY OFFSET)



- Interfaces are laterally offset.
- Uses more area.
- Can reduce interface concentration.

STACKED (VERTICALLY ALIGNED)



- Compact vertical column.
- Filled interfaces and target lands require careful process and reliability control.
- More sensitive to alignment, voids and copper balance.

A microvia is not automatically more reliable.

COST FOLLOWS THE BUILD



THROUGH VIAS ONLY
- Conventional lamination.
- Standard drilling and plating.
- Lowest complexity and cost.



ONE-LEVEL MICROVIA
- Requires laser drilling.
- Fill and plate microvias.
- Added process and cost.



BURIED + MICROVIA
- Uses subassembly cores.
- Sequential build-up required.
- Higher complexity and cost.



MULTIPLE STACKED LEVELS
- Repeated build-up interfaces.
- Tight process window.
- Highest complexity and risk.

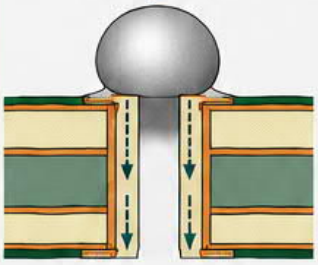
Minimize stacked levels. Consider staggered vias, layer reassignment, fan-out changes or a different stack-up first.

VIA TYPES AND MANUFACTURING CONSIDERATIONS

VIA-IN-PAD • FILLING • THERMAL DESIGN

OPEN VIA-IN-PAD

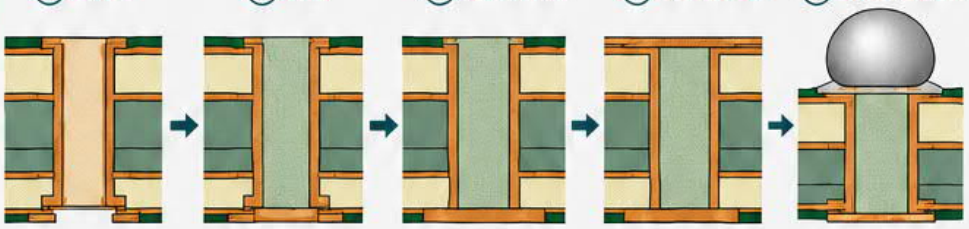
Solder drains into the hole and wicks along the barrel.



Reduced solder volume and higher voiding risk.

FILLED, PLANARIZED & CAPPED VIA-IN-PAD

Maintains solder volume, stand-off and reliability under a BGA.

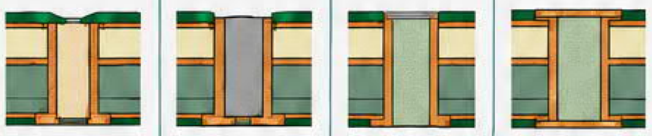


① PLATE	② FILL	③ PLANARIZE	④ COPPER CAP	⑤ FINISHED LAND
Via plated per design.	Fill cavity with approved material.	Remove excess and achieve flat surface.	Plate copper onto planar surface.	Solderable land ready for assembly with full solder volume and stand-off.

Copper | Prepreg (Dielectric) | Core (Dielectric) | Solder Mask | Fill Material | Copper Cap

TERMINOLOGY MATTERS

*Via-in-pad, filled via, capped via and **VIPPO** are related but not interchangeable.*



TENTED	PLUGGED	FILLED	CAPPED / PLATED OVER
• Solder mask covers the opening. • Cavity not filled.	• Material intentionally closes or partly fills the hole. • May not be planar.	• Cavity filled with a defined material or process. • Surface may require planarization.	• Copper plated over filled, planarized via. • Provides a solderable land at final surface.

FILL OPTIONS



NONCONDUCTIVE EPOXY – Common for planarization/VIPPO; provides flat surface for solderable land. Copper barrel carries current.



CONDUCTIVE FILL – Specialized use; material, CTE and reliability must be qualified for the application.



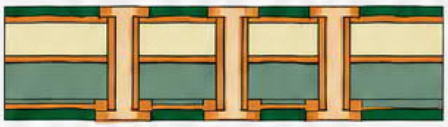
COPPER-FILLED MICROVIA – Supports stacking and high-density routing; fill and interface integrity are critical.



OPEN VIA – Lowest complexity and cost; unsuitable beneath many solderable pads and for high-reliability assemblies.

POWER VIAS

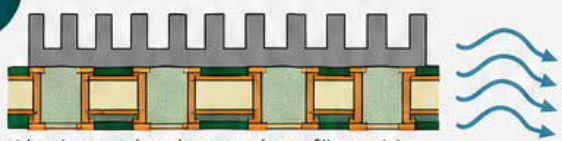
Use parallel vias and a complete power delivery strategy.



- *Use multiple vias in parallel to share current.*
- *Design for sufficient barrel copper, finished geometry and plating integrity.*
- *Consider current sharing, plane connections, and temperature rise through the stack.*
- *Do not rely on simple "amp-per-via" rules.*

THERMAL VIAS

Evaluate the entire heat path – not just the via.



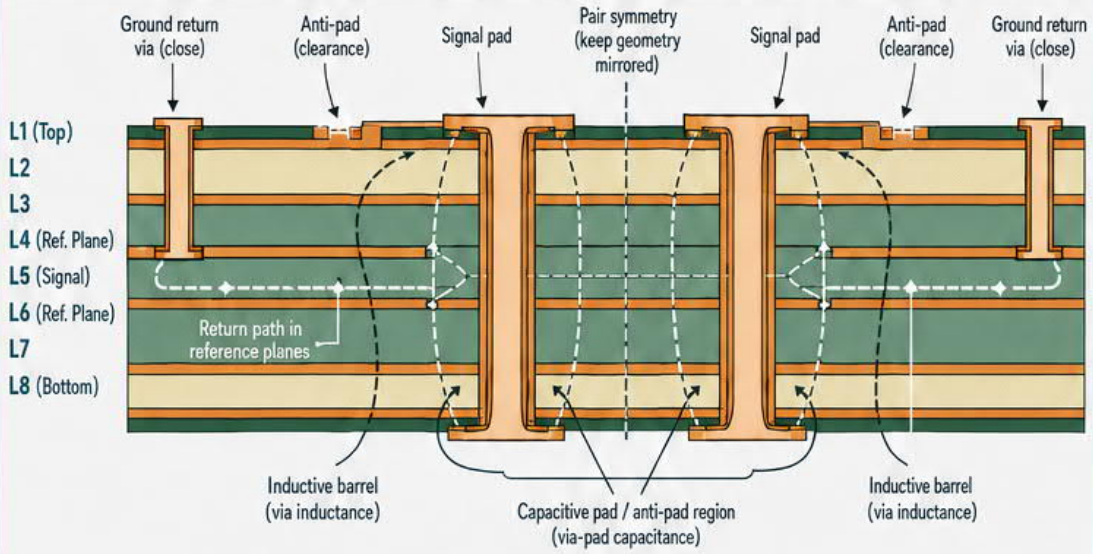
- *Consider via count, barrel copper, planes, fill material, heatsink, and airflow as one thermal system.*
- *Ensure strong thermal coupling to planes and heatsink.*
- *Control solder wicking to preserve solder volume and component stand-off.*
- *Validate with thermal analysis and real-world testing.*

An open via beneath a solderable pad *can reduce solder volume, increase voiding and upset component stand-off.*

VIA TYPES AND MANUFACTURING CONSIDERATIONS

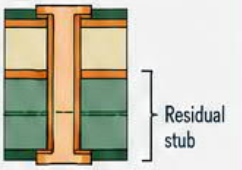
HIGH-SPEED • BACKDRILL • RETURN PATHS

DIFFERENTIAL VIA TRANSITION THROUGH A MULTILAYER PCB



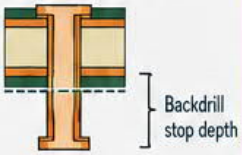
UNUSED BARREL STUB

Unconnected barrel below last signal layer creates an inductive stub.



OPTIONAL BACKDRILL

Backdrill removes unused barrel below target depth.



KEY DESIGN LEVERS

MINIMIZE UNNECESSARY VIA LENGTH AND STUB
Shorter is better for loss, reflections and crosstalk.

ENGINEER ANTI-PAD GEOMETRY
Balance capacitance, clearance and manufacturability.

PLACE RETURN / STITCHING VIAS CLOSE
Minimize loop area and return inductance.

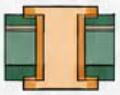
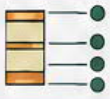
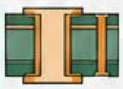
KEEP DIFFERENTIAL STRUCTURES SYMMETRIC
Include pads, anti-pads, vias, and reference vias.

REMOVE NONFUNCTIONAL PADS ONLY WHEN ANALYSIS / PROCESS ALLOWS
Avoid increased mode conversion and impedance steps.

CONSIDER BLIND / MICROVIA OR BACKDRILL
Use when channel analysis shows benefit.

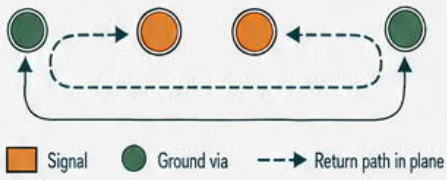
USE 3D EM ANALYSIS FOR VERY HIGH-SPEED / RF LAUNCHES
Validate transitions, stubs and return paths with full-wave tools.

BACKDRILL DRAWING CONTROLS

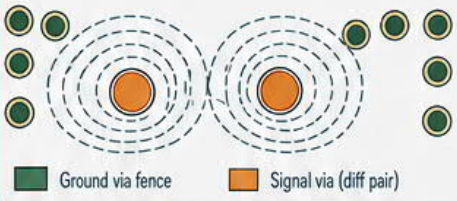
CONTROL	DESCRIPTION / GUIDANCE
	**AFFECTED VIAS** Specify which vias are to be backdrilled (IDs or classes).
	**DRILL SIDE** Indicate from Top, Bottom or Both sides.
	**START / STOP LAYER OR TARGET DEPTH** Define the last functional layer or target depth to stop drilling.
	**MAXIMUM RESIDUAL STUB** Specify maximum allowed stub length after backdrill.
	**DIAMETER / CLEARANCE** Backdrill diameter (finished) and required clearance to adjacent copper.
	**REGISTRATION** Tight positional tolerance between original via and backdrill.
	**INTERNAL NONFUNCTIONAL-PAD BREAKTHROUGH** Indicate if internal pads may be broken through (yes / no).

GROUND STITCHING & SHIELDING

COMPACT RETURN PATHS
Keep return vias close to the signal vias.
Minimize loop area between signal and return.



PLANE CONNECTION & VIA FENCES
Use via fences to contain fields, prevent mode conversion and reduce radiation.



SPACING IS ELECTROMAGNETIC, NOT VISUAL
Set spacing and density based on impedance control, field containment and return current behavior — not on visual patterns or marketing rules.

Backdrill must be driven by channel analysis and stub length — not data-rate marketing numbers alone.

Differential pair symmetry includes vias, anti-pads, planes and reference vias.

CONTROL, QUALIFY AND RELEASE

CONTROL • QUALIFICATION • RELEASE

1. PURPOSE
2. VIA ARCHITECTURE
3. FABRICATOR CAPABILITY
4. CONTROLLED DRAWING
5. REPRESENTATIVE COUPON
6. THERMAL / REFLOW TEST
7. MICROSECTION + RESISTANCE EVIDENCE
8. RELEASE

FABRICATION DRAWING – DEFINE

PTH	finished hole, pad, plating / performance requirement.
BLIND / BURIED	start layer, stop layer, hole and build sequence.
MICROVIA	layer pair, diameter / pad, fill, stacked or staggered.
VIA-IN-PAD	fill, planarize and cap / plated-over condition.
BACKDRILL	side, affected vias, depth / stop, residual stub and diameter.
PRESS-FIT	connector-specific finished hole / tolerance and plating.
PROTECTED VIA	tented, plugged, filled or capped finished condition.

RELIABILITY EVIDENCE

MICROSECTION – BARREL PLATING AND INTERFACES
Uniform copper thickness, complete coverage and sound copper-to-copper interfaces.

REGISTRATION
Layer-to-layer alignment within process capability.

MICROVIA TARGET-PAD INTERFACE
Adequate land, centered via, no breakout or pad lift.

FILL / VOIDS (AS APPLICABLE)
Voids within limits or fully filled as specified.

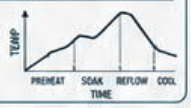
BACKDRILL RESIDUAL STUB
Measured stub length within specification.

REPRESENTATIVE VIA-CHAIN COUPONS
Test worst-case structures and longest signal paths.

LOT / PANEL TRACEABILITY
Coupon ID linked to panel/lot, process parameters and inspection records.

COUPON ID
12345-ABC-01

THERMAL / REFLOW RESISTANCE MONITORING
Controlled thermal profile and monitoring: pass/fail criteria met.



COMMON MISTAKES

- ✗ Smallest advertised via.
- ✗ Ignored aspect ratio.
- ✗ Open pad via.
- ✗ Many stacked levels.
- ✗ No return vias.
- ✗ Ignored stub.
- ✗ Vague "filled via".
- ✗ Manual drill compensation.
- ✗ Tiny pads without registration margin.
- ✗ No representative coupons.
- ✗ Too many special processes without early DFM.

A visually acceptable microsection may not be sufficient evidence for a complex high-reliability microvia structure.

FINAL RELEASE CHECK

SIMPLEST ARCHITECTURE USED
Use the least complex structure that meets the performance requirement.

QUALIFIED SUPPLIER WINDOW
Design within the supplier's qualified process window.

HDI BUILD REVIEWED
Layer build, sequence and materials reviewed and approved.

STACKED LEVELS MINIMIZED
Minimize stacked microvias and total via levels to reduce risk.

CURRENT/THERMAL/HIGH-SPEED NEEDS ASSESSED
Verify current, thermal and signal integrity requirements are achieved.

TERMINOLOGY PRECISE
Use accurate, consistent terms and requirements.

DRAWINGS AND COUPONS CONTROLLED
Controlled revision, coupon IDs and change management.

DFM AND CAPABILITY APPROVAL COMPLETE
DFM review and supplier capability approval on file.

Choose the simplest manufacturable architecture and verify critical interconnects with traceable evidence.